WHAT IS CLAIMED IS:

1. A method of writing data, including:

specifying the size of processed data deriving from each data block when a predetermined processing is performed, in parallel, on a plurality of data blocks; and

specifying a write-start address for the plurality of data blocks by calculating addresses based on the size specified by said specifying the size, wherein the write-start address is used when the processed data deriving from each data block is written to a memory.

2. A method according to Claim 1, wherein the predetermined processing is coding.

3. A method according to Claim 2, wherein the coding is variable-length coding.

4. A method according to Claim 1, wherein said specifying a write-start address is such that the processed data deriving from the plurality of data blocks are stored in the memory in a continuous manner at the time when writing the processed data has been completed.

5. A data writing apparatus, including:

an address specifying unit which calculates an address

based on the size of processed data deriving from each data block when a predetermined processing is performed on a plurality of data blocks in parallel, and which specifies a write-start address used when the processed data deriving from each data block are written to a memory, for the plurality of data blocks; and

a write control unit which writes, in parallel, to the memory the processed data deriving from the plurality of data blocks, according to the write-start addresses specified for the plurality of data blocks.

6. A data writing apparatus according to Claim 5, wherein the predetermined processing is coding.

7. A data writing apparatus according to Claim 6, wherein the coding is variable-length coding.

8. A data writing apparatus according to Claim 6, wherein said address specifying unit calculates the amount of coded data deriving from each data block.

9. A data writing apparatus according to Claim 5, wherein said write control unit realizes a state in which the processed data deriving from the plurality of data blocks are stored in the memory in a continuous manner at the time when writing the processed data has been completed.

10. A coding apparatus, including:

a plurality of encoders which perform, in parallel, variable-length coding on a plurality of data blocks; and

an address specifying unit which specifies, based on the amount of coded data generated by said encoders, a write-start address which is used when the coded data are written to a memory, for the plurality of data blocks; and

a write control unit which writes, in parallel, to the memory the processed data deriving from the plurality of data blocks, according to the write-start addresses specified for the plurality of data blocks.

11. A coding apparatus according to Claim 10, wherein said address specifying unit calculates the amount of coded data deriving from each data block.

12. A coding apparatus according to Claim 10, wherein said write control unit realizes a state in which the processed data deriving from the plurality of data blocks are stored in the memory in a continuous manner at the time when writing the processed data has been completed.

13. A digital camera, including:

an image pickup unit;

a mechanism control unit which controls mechanism of

said image pickup unit; and

a processing unit which processes digital images obtained by said image pickup unit,

wherein said processing unit performs coding, in parallel, on a plurality of data blocks that constitute the digital images, and when coded data generated by the coding are written, in parallel, to a memory, said processing unit realizes a state in which the coded data deriving from the plurality of data blocks are stored in the memory in a continuous manner at the time when writing the coded data has been completed.

14. A digital camera according to Claim 13, wherein said processing unit includes:

a plurality of encoders which perform variable-length coding, in parallel, on the plurality of data blocks;

an address specifying unit which specifies, based on the amount of coded data generated by said encoders, a write-start address which is used when the coded data are written to the memory, for the plurality of data blocks; and

a write control unit which writes, in parallel, to the memory the coded data deriving from the plurality of data blocks, according to the write-start addresses specified for the plurality of data blocks.